THE INVENTION CLAIMED IS:

1. A method of selecting a signal from a plurality of signals comprising:

providing a plurality of multiplexers, each multiplexer adapted to selectively output one of a plurality of input signals input by the multiplexer using an output of the multiplexer;

selecting an input signal from one of the plurality of multiplexers to output;

outputting the selected input signal from the output of the one of the plurality of multiplexers;

forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state; and

combining the outputs of the plurality of multiplexers so as to output the selected input signal.

2. The method of claim 1 wherein selecting the input signal from one of the plurality of multiplexers to output includes:

generating a plurality of select signals; and

providing a unique portion of the select signals to each of the plurality of multiplexers.

3. The method of claim 2 wherein generating the plurality of select signals includes generating select signals, wherein only one of the select signals is of a high logic state.

4. The method of claim 1 wherein forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state includes:

generating a plurality of activation signals to activate one of a pull-up circuit and a pull-down circuit in the other of the plurality of multiplexers; and

forcing the outputs of the other of the plurality of multiplexers to the predetermined logic state using the one of the pull-up circuit and the pull-down circuit.

5. The method of claim 1 wherein outputting the selected input signal from the output of the one of the plurality of multiplexers, and forcing the outputs of the other of the plurality of multiplexers to a predetermined logic state are performed in parallel.

6. The method of claim 1 wherein combining the outputs of the plurality of multiplexers comprises employing one of a logic OR and a logic AND operation to combine the outputs of the plurality of multiplexers.

7. A multiplexer circuit adapted to select a signal from a plurality of signals comprising:

a plurality of multiplexers, each multiplexer adapted to selectively output one of a plurality of signals input by the multiplexer using an output of the multiplexer;

a first decoder circuit coupled to the plurality of multiplexers and adapted to generate a plurality of select signals to select an input signal from one of the plurality of multiplexers to output;

a second decoder circuit coupled to the plurality of multiplexers and adapted to generate a plurality of activation signals to force the outputs of the other of the plurality of multiplexers to a predetermined logic state; and

a logic circuit coupled to the plurality of multiplexers and adapted to combine the outputs of the plurality of multiplexers so as to output the selected input signal.

8. The multiplexer circuit of claim 7 wherein each of the plurality of activation signals correspond to a different one of the plurality of multiplexers.

9. The multiplexer circuit of claim 7 wherein the first and second decoder circuits employ a common input to generate the plurality of select signals and the plurality of activation signals.

10. The multiplexer circuit of claim 7 wherein the first and second decoder circuits operate in parallel.

11. The multiplexer circuit of claim 7 wherein the logic circuit is adapted to perform an AND operation on the outputs of the plurality of multiplexers.

12. The multiplexer circuit of claim 7 wherein the logic circuit is adapted to perform an OR operation on the outputs of the plurality of multiplexers.

13. The multiplexer circuit of claim 7 wherein the first decoder circuit is further adapted to output a

unique portion of the select signals to each of the plurality of multiplexers.

14. The multiplexer circuit of claim 13 wherein the plurality of select signals and the plurality of input signals input by each of the plurality of multiplexers have an equal number.

15. The multiplexer circuit of claim 7 wherein the first decoder circuit is further adapted to generate a plurality of select signals, wherein only one of the plurality of select signals is of a high logic state.

16. The multiplexer circuit of claim 7 wherein each of the plurality of multiplexers includes a pull-up circuit; and

wherein the second decoder circuit is further adapted to:

generate a plurality of activation signals to activate the pull-up circuits coupled to the other of the plurality of multiplexers; and

force the outputs of the other of the plurality of multiplexers to the predetermined logic state using the pull-up circuits coupled to the other of the plurality of multiplexers.

17. The multiplexer circuit of claim 16 wherein the logic circuit is adapted to perform an AND operation on the outputs of the plurality of multiplexers.

18. The multiplexer circuit of claim 7 wherein each of the plurality of multiplexers includes a pull-down circuit; and

wherein the second decoder circuit is further adapted to:

generate a plurality of activation signals to activate the pull-down circuits coupled to the other of the plurality of multiplexers; and

force the outputs of the other of the plurality of multiplexers to the predetermined logic state using the pull-down circuits coupled to the other of the plurality of multiplexers.

19. The multiplexer circuit of claim 18 wherein the logic circuit is adapted to perform an OR operation on the outputs of the plurality of multiplexers.